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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,298	04/23/2001	Michitaka Urushima	NEC01P030-HSc	3167

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McGinn & Gibb,PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817

EXAMINER
GEYER, SCOTT B

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/839,298	Applicant(s) URUSHIMA, MICHITAKA	
	Examiner Scott B. Geyer	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,25,26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 25* is/are allowed.

6)☒ Claim(s) *1-7,9,26 and 28-31* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The references cited within the information disclosure statement, entered as paper no. 9, have been considered.

Drawings

2. Claim 27 has been cancelled by the applicant. Therefore, the objection to the drawings from the previous office action is withdrawn.

Claim Rejections - 35 USC § 112

3. Claim 30 as amended by the applicant is acceptable; the rejection of claim 30 under 35 USC 112 first and second paragraphs has been overcome by the amendment.

4. Claim 27 has been cancelled rendering the rejection under 35 USC 112 second paragraph moot.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Yasumoto et al. (4,612,083).

As to ***claim 7***, Yasumoto et al. teach two semiconductor devices 10 and 10' in figure 1(e). Each device comprises a chip (semiconductor element) 14 (and 14') with internal conductor layers (bond pads) 18 (and 18'). An adhesive resin layer 22 (and 22') is provided on a surface of each chip and metal bumps 20 (and 20') are provided through the adhesive layer. The metal bumps are exposed at the outer surface of the

adhesive layer. The two outer surfaces (the adhesive resin surfaces) are mated together as shown in figure 1(f) such that the metal bumps contact each other for electrical connection and the adhesive resin layers contact each other for physical connection and bonding.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1, 9, 26, 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima (JP 05-003183) in view of Hayes (6,114,187).

As to ***claim 1***, Urushima teach a chip substrate 4, stud bumps 10 on the chip substrate, a protective film 12 on the chip substrate (on the same surface as the stud bumps 10) and wherein the stud bumps 10 are exposed on the surface of the adhesive layer (see figure 1). Further, Urushima teach the protective film layer to be a layer of cured epoxy resin, which is an adhesive layer. Urushima does not specifically teach stud bumps which project from the adhesive layer surface. However, Hayes teaches a similar structure in figures 4c and 4d wherein solder columns extend from pads 2 on a chip 1. A dielectric layer 30 is applied to the active surface of the chip, yet the solder columns still project from the surface of the dielectric layer. Further, in figure 4d, the solder columns are changed to bumps 21, yet the bumps also project above the surface of the dielectric layer. Therefore, it would have been obvious to a person of ordinary skill in the art to modify the device of Urushima with stud bumps which project above the surface of an adhesion layer as taught by Hayes so as to provide an extended feature

which will assure electrical connection to other chips or circuit boards through bonding techniques, such as flip-chip bonding.

As to ***claim 9***, Urushima teach the adhesive layer composed of a cured epoxy resin (see abstract).

As to ***claim 26***, Hayes teach in figure 4d, a protruding stud bump 21, as was also stated above in the rejection of claim 1.

As to ***claim 28***, the examiner takes official notice on the language of claim 18 wherein "stud bump comprises gold", since it is well known in the art of semiconductor devices and semiconductor manufacturing to have stud bumps made of gold.

As to ***claim 29***, Urushima teach the protective film to be an epoxy resin which is cured (see abstract).

As to ***claim 31***, Urushima teaches stud bums 10 attached to the electrodes 11. Further, as to claim 31 which recites that the stud bump is "connected to said electrode via an ultrasonic weld", this limitation has not been given patentable weight, as the method limitation does not give breadth or scope and fails to further limit the product claim.

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9. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima (JP 05-003183) and Hayes (6,114,187) as applied to claim 1 above, and further in view of applicant's admitted prior art.

As to ***claim 2***, neither Urushima nor Hayes teach an interposer attached to the device of claim 1. However, applicant's admitted prior art teach a similar device in

figure 3 wherein the chip is attached to an interposer. Further, as to claim 2 which recites that the interposer is "bonded through thermocompression bonding", this limitation has not been given patentable weight, as the method limitation does not give breadth or scope and fails to further limit the product claim. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Urushima and Hayes with an interposer as is taught by applicant's prior art so as to provide a suitable platform for attachment of the chip to another substrate, i.e. mother board or circuit board.

As to ***claim 4***, applicant's prior art figure 3 teaches an interposer (72B) with a device hole (96).

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10. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Capote et al. (1998 International Symposium on Advanced Packaging Materials).

As to ***claim 3***, applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d) and applicant's prior art figure 3 teaches a chip (70) with bumps (80) to be attached to an interposer (72B). Applicant's admitted prior art does not specifically teach a cured flux. However, Capote et al. teach the use of fluxes in flip chip bonding of chips to substrates. Capote et al. further teach that the flux will be cured after re-flow of the solder balls is completed (see pages 6 and 7). At the time of the invention, it would have been obvious to a person of ordinary skill

in the art to modify the device of applicant's admitted prior art with a flux as taught by Capote et al. so as to assist in the re-flow of the solder balls for proper attachment of the chip to the substrate, i.e. interposer.

As to ***claim 6***, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98), which can be a resin layer (applicant's disclosure, page 4, lines 3-16) on the surface of a chip and allowing bumps (80) to be exposed and electrically attach to a wiring pattern on an interposer (72B). The wiring pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls. Applicant's admitted prior art does not specifically teach a cured flux. However, Capote et al. teach the use of fluxes in flip chip bonding of chips to substrates. Capote et al. further teach that the flux will be cured after re-flow of the solder balls is completed (see pages 6 and 7). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of applicant's admitted prior art with a flux as taught by Capote et al. so as to assist in the re-flow of the solder balls for proper attachment of the chip to the substrate, i.e. interposer.

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11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Hayes (6,114,187).

As to ***claim 5***, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98) on the surface of a chip and allowing bumps (80) to be exposed and electrically attach to a wiring pattern on an interposer (72B). The wiring

pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls. Applicant's prior art does not specifically teach stud bumps which project from the adhesive layer surface. However, Hayes teaches a similar structure in figures 4c and 4d wherein solder columns extend from pads 2 on a chip 1. A dielectric layer 30 is applied to the active surface of the chip, yet the solder columns still project from the surface of the dielectric layer. Further, in figure 4d, the solder columns are changed to bumps 21, yet the bumps also project above the surface of the dielectric layer. Therefore, it would have been obvious to a person of ordinary skill in the art to modify the device of Urushima with stud bumps which project above the surface of an adhesion layer as taught by Hayes so as to provide an extended feature which will assure electrical connection to other chips or circuit boards through bonding techniques, such as flip-chip bonding.

Response to Arguments

12. Applicant's arguments with respect to claims 1, 5, 7, 26 and 28 have been considered but are moot in view of the new ground(s) of rejection.

13. No argument was presented by the applicant with respect to the subject matter contained within dependent claims 2, 4, 9, 29 and 31. Therefore, the rejections of these claims have been repeated.

14. The applicant has argued (on pages 9 and 10 of the response), with respect to claims 3 and 6 that the applied reference does not teach the claimed invention as it pertains to the bumps projecting from a surface of the protection resin layer (see

specifically the last paragraph of page 10 of the response). However, neither claim 3 nor claim 6 recite a bump which "projects" from the surface, as related to the definition of "project" supplied by the applicant. Instead, both of these claims recite bumps which are "exposed", which is clearly met by the cited references. Applicant should note that the examiner has provided a secondary reference for "projecting bumps" for amended claims 5 and 7, and also for claim 1, which will be applied in the next office action if the applicant sees fit to amend either claim 3 or claim 6 to include the limitation of "project" rather than "exposed".

As to applicant's assertion throughout the response, specifically to the cited prior art references applied relating to entirely different subject matter, the applicant is directed to the following:

In response to applicant's argument that the cited references are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, all of the cited references are in filed of the applicant's endeavor, specifically semiconductor devices. Therefore, all of the cited references are valid, analogous and one of ordinary skill in the art would have been apprised of them. Furthermore, the mere stating of the particulars of each reference as a basis for a nonanalogous argument is not reason enough to invalidate the reference.

Allowable Subject Matter

15. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention wherein the device of claim 1 has an adhesion layer comprised of a thermoplastic resin which also has a thickness of 50 micrometers.

16. Claims 8 and 25 are allowed.

17. The following is a statement of reasons for the indication of allowable subject matter: reasons.

Conclusion

18. This action is **NON-FINAL**, due to newly added references not entirely dependent upon applicant's amending of claims.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

S.B.G.

S.B.G.
February 13, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800